Design and Implementation of Resonant Tunneling Devices into Circuits and Applications

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For the year 2010, the Semiconductor Industry Association Roadmap[1] projects a minimum gate length for MOS transistors of 0.07 μm. Advances in heterostructure epitaxial growth have created a vast range of possible material systems that can be used for nanoscale device design in the vertical (growth) dimension. Future device designers will be concerned about the quantum mechanical character of the carriers confined in nanoscale semiconductor devices. A paradigm shift will be required when this quantum mechanical character can no longer be circumvented by smart designs. Quantum mechanical effects will then be exploited to enhance device performance. This presentation will highlight some of TI's recent advances in material, device and circuit research in the area of Nanolelectronics. Topics discussed in particular will be computer aided design tools, Si/SiO_2 tunneling, analog to digital converters, and memory cells.

To drive the rapid development and analysis of quantum devices we have implemented a comprehensive 1-D quantum device simulator that incorporates the effects of charging, multiple bands, and scattering for arbitrary layer compositions in the III/V and Si material system. This Nanoelectronic Modeling Tool (NEMO[2–4]) is designed to provide rapid turn-around for a device designer and detailed analysis for a device physicist. Within a graphical user interface a large set of models can be analyzed and compared. Work on a 2-D simulator is under way.

This simulator is presently used to guide the development of Si resonant tunneling diodes (RTD). Figure 1 shows the good agreement between the NEMO simulation and experimental[5] tunneling currents through ultrathin SiO_2 barriers as a function of bias for several oxide thicknesses.

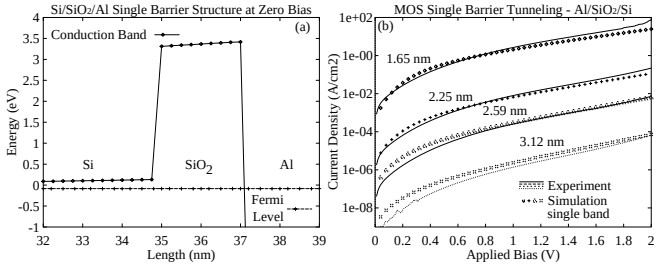

FIG. 1. (a) Conduction band edge and Fermi-level of one of the single barrier structures at zero bias. (b) Experimental and simulated tunneling current at 300K through a single SiO_2 barrier for different barrier thicknesses.

Integration of III/V RTD's onto Si substrates has been shown in reference [6]. Compound semiconductor RTD designs are now being optimized for high speed GaAs and InP Analog to Digital Converters (ADC), shift registers, and memory, where both high and low current designs are needed. Figure 2a compares a full band (sp3s*) NEMO simulation[7] of a high current density InP based strained InGaAs/AlAs RTD at 300K to experimental results. Experimental results for a low current density GaAs/AlAs RTD at 4.2K are compared to a simulation including scattering due to polar optical phonons, acoustic phonons, and interface roughness in Figure 2b.

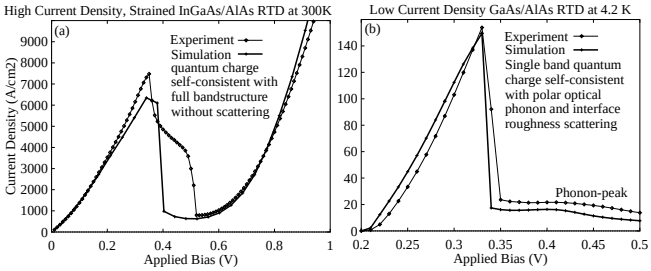

FIG. 2. Experimental and simulated current voltage characteristics for two different RTD's.

To incorporate InP-based RTD's into compact circuits, an integrated process for HFET's and RTD's has been developed. We recently demonstrated[8] a record 50 nano Watt III/V **T**unneling-based **SRAM** cell which combines a ultra-low current density RTD's[9] and heterostructure field effect transistors (HFET). The TSRAM test cell and the waveforms of the HFET/RTD are plotted in Figure 3. Work on integrated high speed GaAs and InP ADC's is also under way.

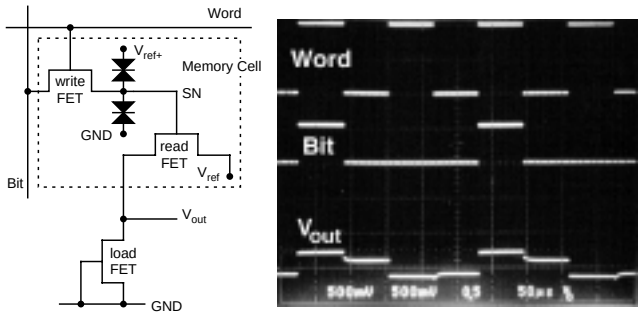

FIG. 3. TSRAM cell test circuit and Waveform of the HFET/RTD TSRAM cell. Input levels (from top to bottom): word line 0,-1 V; bit line 0,0.55 V. RTD latch bias is 0.45 V. V_{out} represents the storage node voltage that latches to stable "0" and "1" levels defined by low current density RTD's. Cell power is 50 nano Watt.

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